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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/668,817	09/22/2003	David Zimmerman	42P16614	1962

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EXAMINER	
LAU, TUNG S	

ART UNIT	PAPER NUMBER
2863	

DATE MAILED: 01/21/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/668,817	ZIMMERMAN ET AL.	
	Examiner	Art Unit	
	Tung S Lau	2863	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *23 December 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *5-13* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *5-13* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *See office action*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Information Disclosure Statement

1. Information Disclosure Statement filed on 12-22-2003 is acknowledged by the examiner; A copy of a signed PTO-1449 attached with this office action.

Election/Restrictions

2. A response on 12-23-2004 a provisional election was made **without traverse** to prosecute the invention of claims 5-13. Claims 1-4 and 14-21 are cancel. Applicant is reminded that upon the cancellation of claims to a non-elected invention, the inventorship must be amended in compliance with 37 CFR 1.48(b) if one or more of the currently named inventors is no longer an inventor of at least one claim remaining in the application. Any amendment of inventorship must be accompanied by a request under 37 CFR 1.48(b) and by the fee required under 37 CFR 1.17(i).

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 5-13 are rejected under 35 U.S.C. 102(b) as being anticipated by Hii et al. (U.S. Patent Application Publication 2002/0089887).

Regarding claim 5:

Hii discloses a memory integrated circuit (IC) module, comprising: a carrier substrate (abstract, fig. 1); a plurality of first and second signal connection points being installed on the substrate (page 1, section 0002-005); a plurality of memory devices installed on the substrate (fig. 5, unit 240), each of which has a separate memory core array and separate address decoder logic (fig. 1, unit 200, 240, fig. 3, unit 340, 370); and a memory buffer installed on the substrate and communicatively coupled between the plurality of first and second signal connection points and the plurality of memory devices (fig. 13a-c, fig. 1, unit 100, 125), the buffer having a plurality of driver circuits whose outputs are coupled to the plurality of first signal connection points (fig. 13a-c), respectively, and logic to a) forward read data, provided by the plurality of memory devices (fig. 1, unit 100, 120), at speed using the plurality of drivers in a normal mode of operation for the module (fig. 1, unit 110) and b) determine error in test symbols received from outside the module at speed using the plurality of second signal connection points in a test mode of operation for the module during which a chip-to-chip connection between the module and another device is tested (page 9, unit 0215-260).

Regarding claim 9:

Hii discloses a system of integrated circuit (IC) devices, comprising:

a carrier substrate (abstract, fig. 1); a host IC device having memory controller logic and being installed on the substrate (page 1, section 0002-005), the host IC device having built-in self test (BIST) generator logic coupled between a plurality

of driver circuits and the memory controller logic (fig. 1, unit 200, 240, fig. 3, unit 340, 370), to a) transmit, at speed, address and command information generated by the controller logic, using the plurality of driver circuits in a normal mode of operation for the IC device *fig. 1, unit 200, 240) and b) transmit, at speed, test symbols (fig. 28), using the plurality of driver circuits in a test mode of operation for the IC device during which an interconnect between the IC device and another device is tested (fig. 4, unit 420, 410, 400), the host IC device having BIST checker logic coupled between a plurality of receiver circuits and the memory controller logic (fig. 2, unit 240, fig. 4, unit 430), to a) forward data, received by the plurality of receiver circuits, to the memory controller logic in said normal mode of operation for the IC device and b) determine error in test symbols received by the plurality of receiver circuits in a test mode of operation for the IC device during which an interconnect between the IC device and another device is tested (fig. 4, unit 420, 430, 140); and a first main memory module being installed on the substrate to communicate with the host IC device, the first module having a memory buffer circuit with repeater capability to a) forward address and command information from the memory controller logic to a second main memory module (fig. 2, unit 240), and b) forward read data from the second main memory module to the memory controller logic (fig. 1, unit 130), the first module having first BIST checker logic to determine error in the test symbols transmitted by the BIST generator logic of the host IC device (page 9, unit 0215-260).

Regarding claim 6, Hii further discloses using of DRAM in the test (page 1, section 0020); Regarding claim 7, Hii further discloses a plurality of third and fourth signal connection points being installed on the substrate (abstract, fig. 1, unit 100, 120); and wherein the buffer device includes a further plurality of driver circuits whose outputs are coupled to the plurality of third signal connection points (fig. 1, unit 100, 120), respectively, and further logic to a) forward address and command information, that has been received from outside the module (fig. 1, unit 100, 120), at speed using the further plurality of driver circuits (fig. 1, unit 110) and b) determine error in test symbols, that have been received from outside the module at speed via the plurality of fourth signal connection points, in a test mode of operation module (fig. 1, unit 135); Regarding claim 8, Hii further discloses to decode local memory command, address and data and send to plurality of memory devices (fig. 1, unit 130);); Regarding claim 10, Hii further discloses the second main memory module installed on the substrate to communicate with the host IC device through the first main memory module (fig. 3, unit 340), the second module to re-transmit the test symbols transmitted by the host IC device and forwarded by the first module, back to the first module (fig. 3, unit 340); Regarding claim 11, Hii further discloses second BIST checker logic to determine error in the re-transmitted test symbols received from the second module (page 9, unit 0215-260); Regarding claim 12, Hii further discloses processor main memory to access memory (fig. 2, unit 240, fig. 1, unit 130);

Regarding claim 13, Hii further discloses system chipset for peripherals (fig. 1, unit 135, 115, fig. 2, unit 200, 210).

4. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tung S Lau whose telephone number is 571-272-2274. The examiner can normally be reached on M-F 9-5:30. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, John Barlow can be reached on 571-272-2269. The fax phone numbers for the organization where this application or proceeding is assigned is 703-872-9306 Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

TL

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Supervisory Patent Examiner
Technology Center 2800